WHAT IS CLAIMED IS:

1. A method of configuring a memory apparatus, comprising:

obtaining test information for each of a group of memory locations within the memory apparatus;

compressing the test information to produce compressed test information; and

based on the compressed test information, replacing a group of redundant memory circuits respectively associated with the group of memory locations.

2. The method of Claim 1, wherein said obtaining step includes comparing information stored in said memory locations to respectively corresponding information expected to be stored in said memory locations.

3. The method of Claim 1, wherein the group of memory locations is a group of neighboring memory cells in a DRAM array.

4. The method of Claim 3, wherein the group of neighboring memory cells is a group of adjacent memory cells in a single row of the DRAM array.

5. The method of Claim 1 wherein said compressing step includes storing the test information for each of the memory locations in a corresponding storage location.

6. The method of Claim 5, wherein the test information for each of the memory locations of the group is a corresponding bit which is indicative of whether or not the associated memory location has failed a memory test.

7. The method of Claim 6, wherein said compressing step includes logically combining the stored bits.

8. The method of Claim 7, wherein said logically combining step includes logically ORing the stored bits.

9. The method of Claim 1, wherein said obtaining step includes obtaining test information for each memory location of a plurality of groups of memory locations, said compressing step including compressing the test information respectively associated with each of the groups of memory locations to produce compressed test information.

10. The method of Claim 9, including time division multiplexing the compressed test information for input to a tester that is physically separate from the memory apparatus.

11. The method of Claim 1, wherein said replacing step includes replacing the redundant memory circuits only if the compressed test information indicates that at least one of the group of memory locations has failed.

12. The method of Claim 1, wherein the group of memory locations is a group of neighboring memory cells in a DRAM array, said replacing step including replacing redundant bitlines respectively associated with the neighboring memory cells of the DRAM array.

13, An apparatus for configuring a memory, comprising:

an input for receiving test information for each of a group of memory locations within the memory;

a compression apparatus coupled to said input for compressing the test information to produce compressed test information; and

a replacement apparatus coupled to said compression apparatus and operable based on the compressed test information for replacing a group of redundant memory circuits respectively associated with the group of memory locations.

14. The apparatus of Claim 13, including a compare circuit having an output coupled to said input, having a first input for receiving information stored in said memory locations, and having a second input for receiving corresponding information expected to be stored in said memory locations, said compare circuit operable for comparing said stored information to said corresponding expected information to produce said test information at said output of said compare circuit.

15. The apparatus of Claim 13, wherein said compression apparatus includes storage circuitry having a plurality of storage locations, said storage circuitry coupled to said input for storing the test information for each of the memory locations in a corresponding one of said storage locations.

16. The apparatus of Claim 15, wherein said compression apparatus includes a routing apparatus connected between said input and said storage circuitry for routing the test information for each of the memory locations to its corresponding storage location.

17. The apparatus of Claim 15, wherein the test information for each of the memory locations of the group is a corresponding bit which is indicative of whether or not the associated memory location has failed a memory test.

18. The apparatus of Claim 17, wherein said compression apparatus includes logic coupled to said storage circuitry for logically combining the bits stored in said storage locations.

19. The apparatus of Claim 18, wherein said logic is an OR gate.

20. The apparatus of Claim 13, wherein said input is further for receiving test information for each memory location of a plurality of groups of memory locations, said compression apparatus operable for compressing the test information respectively

associated with each of the groups of memory locations to produce compressed test information.

21. The apparatus of Claim 20, including a multiplexer coupled between said compression apparatus and said replacement apparatus for time division multiplexing the compressed test information for input to said replacement apparatus.

22. The apparatus of Claim 13, wherein said replacement apparatus is operable for replacing the redundant memory circuits only in response to an indication by the compressed test information that at least one of the group of memory locations has failed.

23. The apparatus of Claim 22, wherein said replacement apparatus includes a tester responsive to said compressed test information for determining whether to replace the redundant memory circuits.

24. The apparatus of Claim 13, wherein the group of memory locations is a group of neighboring memory cells of a DRAM array, and wherein the redundant memory circuits are bitlines respectively associated with the neighboring memory cells of the DRAM array.